CLAIMS

What is claimed is:

A sigma-delta converter that includes a feedback loop and operates over a predetermined bandwidth, the sigma-delta converter comprising:

a forward path including:

a summer for generating a first signal;

a filter for averaging the first signal to produce a second signal; and

a comparator for comparing the second signal to a reference level and producing a third signal based on the comparison;

a feedback path providing a representation of the third signal to a negative input of the summer, wherein the summer generates the first signal by subtracting the representation of the third signal from an input signal applied to a positive input of the summer; and

at least one instability generator, positioned in at least one of the forward path and the feedback path, for generating an instability in the feedback loop at a frequency outside the predetermined bandwidth to substantially improve signal-to-noise performance of the sigma-delta converter within the predetermined bandwidth for amplitudes of the input signal that are substantially near a low end of a dynamic range of the sigma-delta converter.

2. The sigma-delta converter of claim 1, wherein the forward path further includes a storage device, coupled to an output of the comparator, for storing the third signal for a delay period and outputting the third signal responsive to a clock signal.

3. The sigma-delta converter of claim 2, wherein the storage device comprises a D flip-flop that outputs the third signal responsive to the clock signal and wherein the at least one instability generator comprises a D flip-flop positioned in the forward path and coupled to an output of the storage device to produce a time-delayed representation of the third signal responsive to the clock signal.

4. The sigma-delta converter of claim 2, wherein sigma-delta converter provides a bandpass frequency response and wherein the storage device comprises:

a first D flip-flop coupled to an output of the comparator and producing an intermediate signal at a non-inverting output responsive to the clock signal; and

a second D flip-flop coupled to the non-inverting output of the first D flip-flop and outputting the third signal at an inverting output responsive to the clock signal.

5. The sigma-delta converter of claim 4, wherein the at least one instability generator comprises at least a third D flip-flop positioned in the forward path and coupled to the inverting output of the second D flip-flop to produce a time-delayed representation of the third signal responsive to the clock signal.

6. The sigma-delta converter of claim 1, wherein the at least one instability generator comprises:

a first D flip-flop responsive to a first edge of a clock signal; and

a second D flip-flop coupled to an output of the first D flip-flop and responsive to a second edge of the clock signal.

7. The sigma-delta converter of claim 1, wherein the at least one instability generator comprises a capacitor.

8. The sigma-delta converter of claim 1, further comprising:

in the forward path:

a second summer for receiving a signal for conversion from a signal source and producing an intermediate signal; and

a second filter, coupled between the summer and the second summer, for averaging the intermediate signal to produce the input signal; and

a second feedback path providing the representation of the third signal to a negative input of the second summer, wherein the second summer produces the intermediate signal by subtracting the representation of the third signal from the signal for conversion.

9. The sigma-delta converter of claim 8, wherein an instability generator of the at least one instability generator is positioned in the second feedback path.

10. An improved sigma-delta converter of the type having at least one feedback loop and operating over a predetermined bandwidth, the at least one feedback loop including a forward path and a feedback path, wherein the improvement comprises:

at least one instability generator, positioned in at least one of the forward path and the feedback path, for generating an instability in the at least one feedback loop at a frequency outside the predetermined bandwidth to substantially improve signal-to-noise performance of the sigma-delta converter within the predetermined bandwidth for amplitudes of an input signal that are substantially near a low end of a dynamic range of the sigma-delta converter.

11. A communication device comprising:

(a) an antenna for receiving a radio signal bearing information;

(b) a receiver, coupled to the antenna, for down-converting and demodulating the radio signal, the receiver including a sigma-delta converter that includes a feedback loop and operates over a predetermined bandwidth, the sigma-delta converter comprising:

a forward path including:

a summer for generating a first signal;

a filter for averaging the first signal to produce a second signal;

a comparator for comparing the second signal to a reference level and producing a third signal based on the comparison; and

a storage device for storing the third signal for a delay period and outputting the third signal responsive to a clock signal to produce a clocked output signal;

a feedback path providing a representation of the clocked output signal to a negative input of the summer, wherein the summer generates the first signal by subtracting the representation of the clocked output signal from a representation of the radio signal applied to a positive input of the summer; and

at least one instability generator, positioned in at least one of the forward path and the feedback path, for generating an instability in the feedback loop at a frequency outside the predetermined bandwidth to substantially improve signal-to-noise performance of the sigma-delta converter within the predetermined bandwidth for amplitudes of the input signal that are substantially near a low end of a dynamic range of the sigma-delta converter;

(c) a clock generator, coupled to the receiver, for generating the clock signal; and

(d) a processor, coupled to the receiver, for decoding and processing the information.

12. The communication device of claim 11, further comprising:

a user input device, coupled to the processor, for receiving user information, wherein the processor encodes the user information; and

a transmitter, coupled to the processor and the antenna, for modulating and upconverting the user information into a transmission signal for transmission from the antenna.

13. The communication device of claim 12, wherein the communication device comprises a two-way radio, a two-way pager, or a radiotelephone.

14. The communication device of claim 11, wherein the communication device comprises a one-way pager.

15. The communication device of claim 11, wherein the storage device comprises a D flip-flop that produces the clocked output signal responsive to the clock signal and wherein the at least one instability generator comprises at least one D flip-flop positioned in the forward path of the feedback loop and coupled to an output of the storage device to produce a time-delayed representation of the clocked output signal responsive to the clock signal.

16. The communication device of claim 11, wherein the at least one instability generator comprises:

a first D flip-flop responsive to a first edge of the clock signal; and

a second D flip-flop coupled to an output of the first D flip-flop and responsive to a second edge of the clock signal.

17. The communication device of claim 11, wherein the sigma-delta converter provides a bandpass frequency response and wherein the storage device comprises:

a first D flip-flop coupled to an output of the comparator and producing an intermediate signal at a non-inverting output responsive to the

clock signal; and

a second D flip-flop coupled to the non-inverting output of the first D flip-flop and producing the clocked output signal at an inverting output responsive to the clock signal.

18. The communication device of claim 17, wherein the at least one instability generator comprises at least a third D flip-flop positioned in the forward path of the feedback loop and coupled to the inverting output of the second D flip-flop to produce a time-delayed representation of the clocked output signal responsive to the clock signal.